CLAIMS

What is claimed is:

1. A processor comprising:

an execution unit; and

a buffer to store data regarding each of a plurality of loads executed by the processor.

2. The processor of claim 1, wherein the buffer is a part of performance monitoring hardware to monitor processor operations.

3. The processor of claim 2, wherein the performance monitoring hardware is to provide data points regarding the executed loads to software.

4. The processor of claim 3, wherein the software is to determine relationships between the executed loads based on the stored data.

5. The processor of claim 1, wherein the buffer comprises a circular buffer.

6. The processor of claim 1, wherein the data stored for each of the plurality of memory operations includes an instruction address.

7. The processor of claim 1, wherein the data stored for each of the plurality of memory operations includes an effective address.

8. The processor of claim 1, further comprising a filter, the filter determining whether the execution of each of the plurality of memory operations meets a criterion for storage.

9. The processor of claim 1, wherein the buffer is to be frozen upon the occurrence of a condition.

10. The processor of claim 9, wherein the condition comprises a miss in a cache, a memory exception, or a programmed event that matches a criterion.

11. A method comprising:

monitoring the execution of a plurality of memory operations by a processor; and

storing information in a buffer regarding the execution of the plurality of memory operations.

12. The method of claim 11, wherein the buffer is implemented in hardware.

13. The method of claim 11, further comprising determining relationships between the executed loads based on the stored information.

14. The method of claim 13, wherein software obtains some or all of the stored information from the buffer and the software is utilized to determine the relationships between the executed loads.

15. The method of claim 11, wherein the stored information includes an instruction address for each of the plurality of memory operations.

16. The method of claim 11, wherein the stored information includes an effective address for each of the plurality of memory operations.

17. The method of claim 11, further comprising determining the base address of a memory operation based on the stored information.

18. The method of claim 11, further comprising deleting the oldest information in the buffer when new information regarding the execution of a load is stored.

19. The method of claim 11, further comprising filtering each of the plurality of memory operations to determine whether to store information regarding the execution of the operation in the buffer.

20. The method of claim 11, further comprising halting the storing of information when a condition is met.

21. The method of claim 20, wherein the condition comprises a cache memory miss, a memory exception, or a programmed event that matches a criterion.

22. A system comprising:

a bus;

a processor coupled to the bus, the processor comprising:

an execution unit;

performance monitoring hardware to monitor operations of the execution unit, the processing monitoring hardware including a buffer to store data regarding each of a plurality of loads executed by the processor; and

a cache memory.

23. The system of claim 22, wherein software is allowed to access the data stored in the buffer.

24. The system of claim 23, wherein the software is to determine relationships between the executed loads based on the stored data.

25. The system of claim 22, wherein the buffer comprises a circular buffer.

26. The system of claim 22, wherein the data stored regarding each of the plurality of loads includes an instruction address.

27. The system of claim 22, wherein the data stored regarding each of the plurality of loads includes an effective address.

28. The system of claim 22, further comprising a filter, the filter determining whether the execution of each of the plurality of loads meets a criterion for storage.

29. The system of claim 22, wherein the operation of the buffer is halted upon the occurrence of a condition.

30. The system of claim 29, wherein the condition comprises a miss in the cache memory, a memory exception, or a programmed event that matches a criterion.